Test pixels for high-temperature infrared scene projection

Christopher J. Fredricksen,[a] Seth Calhoun,[b] Stephen Trewick,[b] Aubrey Coffey,[b] Edward Dein,[b] Kevin R. Coffey,[b] Robert E. Peale,[b,*] Joseph D. LaVeigne,[c] Gregory Franks,[c] Tom Danielson,[c] John M. Lannon,[d] Scott H. Goodwin,[d]

[a]LRC Engineering, Inc. Orlando, FL 32825 (United States), [b]Physics Department, University of Central Florida, Orlando FL 32816 (United States); [c]Santa Barbara Infrared, Inc. 30 S. Calle Cesar Chavez, Suite D, Santa Barbara, CA. 93103 (United States); [d]John M. Lannon, Scott H. Goodwin, RTI International, 3040 E. Cornwallis Rd. RTP, NC 27709 (United States).

ABSTRACT

High pixel temperatures for IR scene projector arrays face materials challenges of oxidation, diffusion, and recrystallization. For cost effective development of new high-temperature materials, we have designed and fabricated simplified pixels for testing. These consist of resistive elements, traces, and bond pads sandwiched between dielectric layers on Si wafers. Processing involves a pad exposure etch, a pixel outline etch, and an undercut etch to thermally isolate the resistive element from the substrate. Test pixels were successfully fabricated by electron-beam lithography using a combination of wet and dry etching.

Keywords: infrared, scene projector, MEMS

1. INTRODUCTION

Infrared scene projection enables realistic simulations of infrared scenes to support hardware-in-the-loop testing of missile seekers, FLIRs, and other imaging systems.[1] Desired higher maximum pixel temperatures[2] are challenged by materials issues such as oxidation of resistive elements, diffusion of impurities into dielectrics with resulting shorts, and strains due to recrystallization. To allow investigation of novel high-temperature materials without the cost of full finished-array manufacturing runs, we have designed and fabricated simplified pixels for testing. Device dies consist of conducting ribbon patterns sandwiched between dielectric layers on Si wafers. The ribbons consist of a resistive heating element connected to probe pads by conducting traces. Processing involves a pad exposure etch, a pixel outline etch, and an undercut etch to thermally isolate the resistive portion of the pixel from the substrate. Test pixels were successfully fabricated by electron-beam lithography using a combination of wet and dry etching.

Fig. 1 presents an image of a typical pixel from a commercial scene projection array. The device consists of multiple patterned layers, comprising different functional elements, and built upon a sacrificial layer that is removed in the final processing step. For the purpose of rapid prototyping and experimentation to reveal unexpected material interactions and device failure mechanisms, leaving time for iterative optimization, we have designed a simplified pixel and processing procedure. Our approach is to fabricate simplified air bridge devices from existing wafer coupons on which dielectric and metal layers have been pre-deposited. The simplified structure comprises a suitable serpentine resistive element with suitable arms and contact pads sandwiched between two blanket layers of suitable dielectric, all supported by a silicon substrate. For these experiments, the contact material was a metal, and the dielectrics layers were a sputtered nitride. The material from which the resistive element is fabricated is a semi-metal and immaterial to the process described here.

*Robert.peale@ucf.edu; phone 407 823-2325; http://www.physics.ucf.edu/~rep/

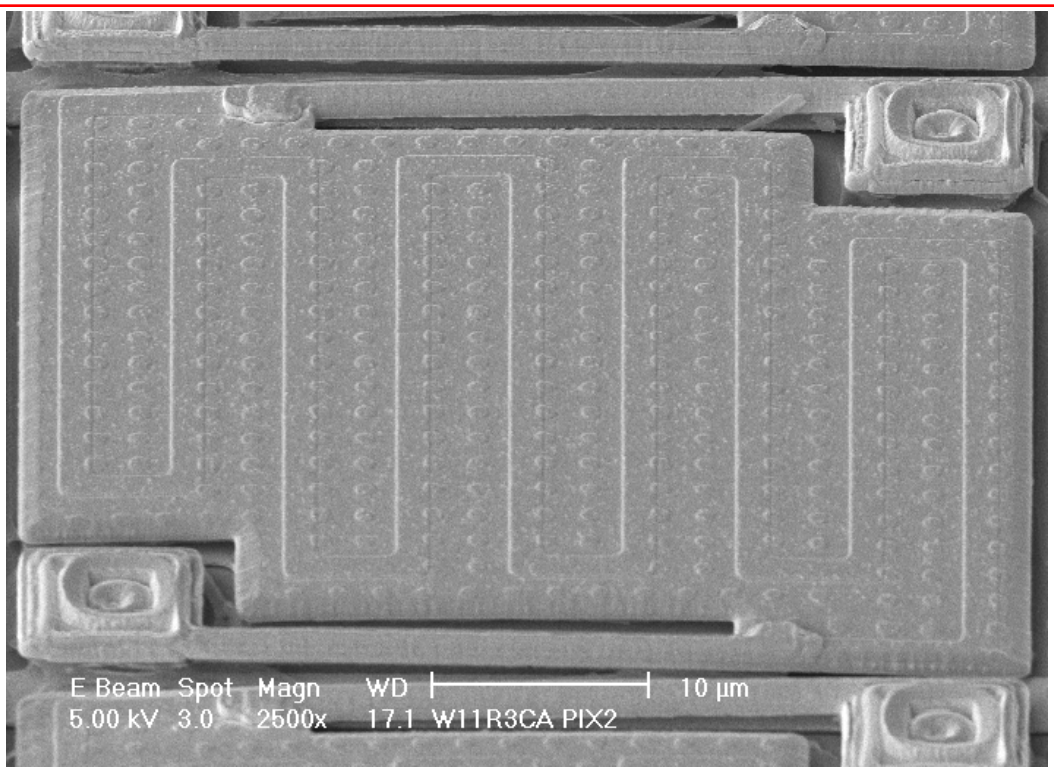

Fig. 1. Example pixel from infrared scene projector array.

2. EXPERIMENT

Wafers with flat serpentine resistors, contact pads, and connecting arms between pads and resistors were sandwiched between nitride layers on silicon by RTI and provided to UCF. Fig. 2 presents schematic illustrations of the process. Firstly, electron-beam resist was spun on the wafers and a pattern was written using a JEOL scanning electron microscope (SEM) with Nabity e-beam writing accessory. A wet etch in KOH exposed the metal contact pads. Secondly, the resist was stripped, and a layer of oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD). A layer of e-beam resist was then spun on. An outline etch pattern was written with the e-beam writer and developed. A dry etch penetrated the oxide, and then a wet etch in KOH cut through the nitride to the silicon. The e-beam resist was stripped. The patterned oxide serves as an etch mask for the subsequent process, protecting both the nitride over the resistor and the metal contact pads. Thirdly, an isotropic dry etch of the silicon in a barrel asher undercut the resistive-element portion of the device to thermally isolate it from the substrate. The remaining oxide mask was removed by a dry etch, which re-exposed the metal contact pads.

Wire bonds were attached to the pads of the finished pixels and the test coupons placed in a small Dewar for testing under vacuum. Tests used a Keithley 2400 source meter to measure current and voltage while driving the pixel. MWIR images of the pixel were simultaneously collected using an IRCameras 800 imager, which had been radiometrically calibrated with a large area blackbody. Pixels were ramped up and down in current over several cycles, with the maximum current increased in each subsequent cycle.

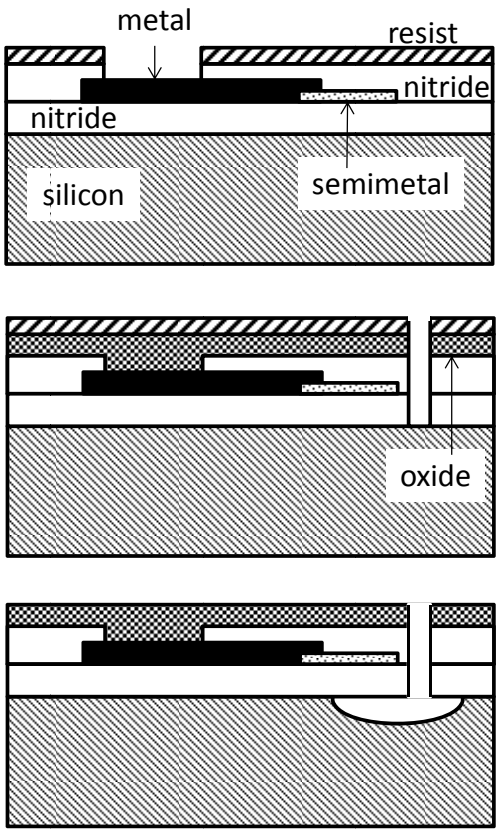

Fig. 2. Schematic illustrations of fabrication process. (Top) pad exposure etch, (middle) outline etch, (bottom), undercut etch.

3. RESULTS

Fig. 3 presents optical microscope images of pixels before and after processing. The metal arms, which are not undercut, lead out of the frame of the images to 200 μm x 200 μm contact pads. Alignment marks (crosses) are apparent. The metal arms connect to thin resistor arms, which begin to be undercut a few microns from the junction. The outline pattern is evident on both sides of the serpentine resistor pattern, and pairs of rectangular vias are evident between each turn of the serpentine to assist in the undercut etch.

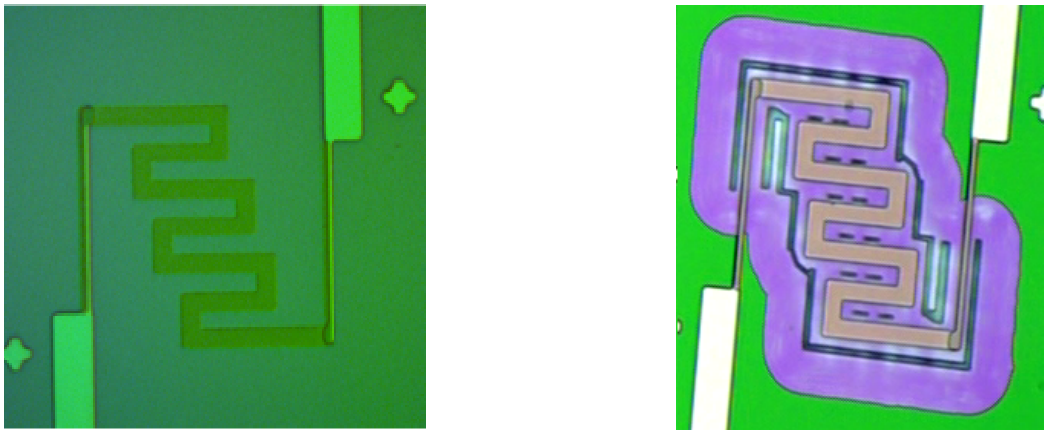

Fig. 3. Optical microscope images of pixels. The left image shows the leg and resistor traces embedded in nitride prior to processing. The right image shows a finished pixelg. 4 presents a scanning electron microscope image of an earlier

undercut experiment. The underlying silicon is etched to a depth of about 5 microns with a rough surface, which is clearly visible through the outline. The central region is nearly free floating in this case, supported mainly by thin arms. However, six bright spots indicate points where the central region may not have been completely released from the silicon, which motivated a change to the pairs of rectangular release holes evident in Fig. 3.

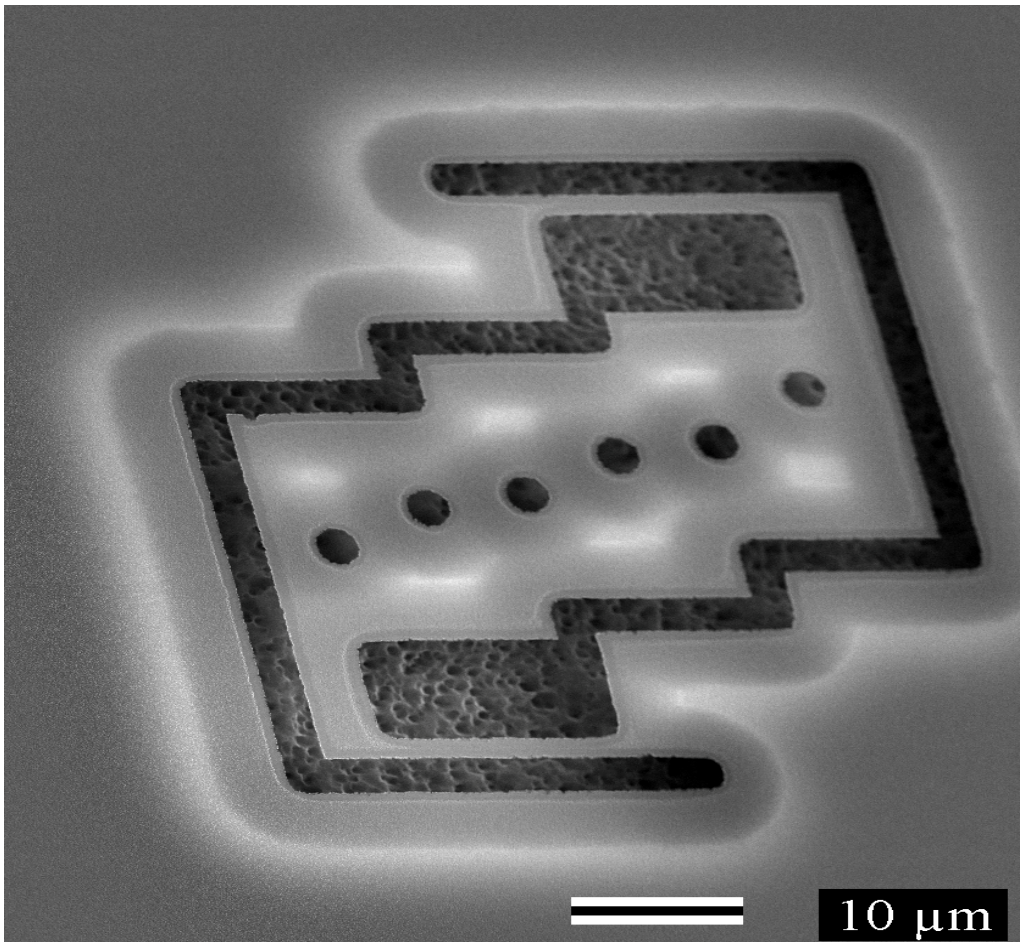

Fig. 4. SEM image of a pixel shaped test pattern from early process optimization. Here the bridge is nearly fully undercut.

Fig. 5 presents data collected from one of current ramps. Pixel voltage, resistance and radiance are shown as a function of test time. Current is ramped up linearly and there is little change in resistance. As the pixel heats, radiance changes rapidly due to the Planck relationship between radiance and temperature. As the pixel cools, the resistance returns to nearly the same value showing little or no annealing during this ramp.

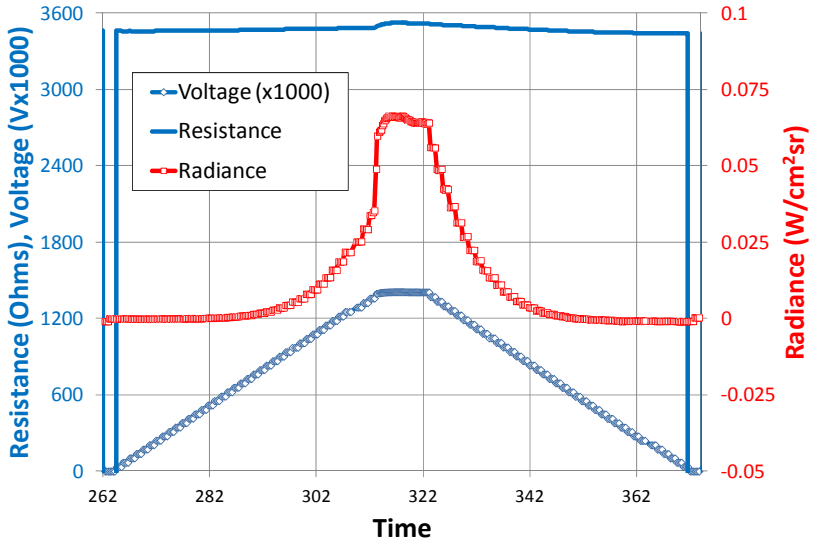

Fig. 5. Single ramp cycle of simplified test pixel

Fig. 6 presents the resistance change as the pixel is heated. Two subsequent ramps in current are included on the plot. Evidence of annealing in the pixel as the radiance increases is that the pixel resistance does not follow the same path up and down on the ramps. On ramp N, the resistance starts a little under 3400 Ohms, rising only slightly as current is applied. Beyond a MWIR radiance of about 0.15 W/cm^2-sr (a little over 650 K apparent temperature) the resistance starts to follow a different curve upwards. Upon cooling it follows a flatter curve down to a different, slightly higher, room temperature value, near 3500 Ohms, indicating some annealing of the resistor is taking place, which is common in these devices. The next time the pixel is heated, it follows the same, flat curve up to a radiance of 0.18 W/cm^2-sr and then again starts to follow a different curve up to about 0.35 W/cm^2-sr. When cooling from there, it follows a flatter path down to a RT resistance just under 4500 Ohms, indicating further annealing.

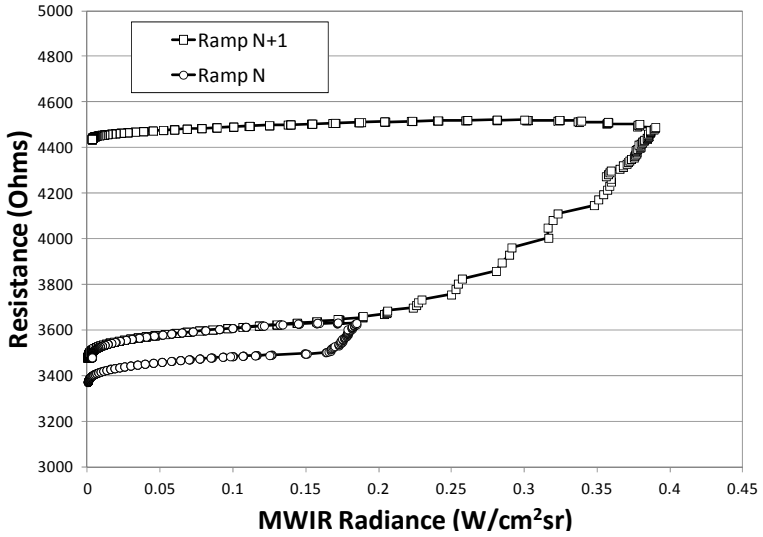

Fig. 6. Pixel resistance vs. average radiance for 2 heating cycles.

Fig. 7 presents radiance vs. applied electrical power for two ramps in current, one in the middle of testing and the final ramp. The lower current ramp up and down and final ramp up all exhibit similar output radiance as a function

of input power. The variations shown are attributable to small changes in emissivity, which is common as pixels anneal at higher temperatures. There is no evidence of thermal shorts developing, which are usually abrupt changes in slope. The pixel fails at a radiance of about 0.7 W/ cm^2-sr, or a MWIR apparent temperature of about 1020 K. After tests, optical micrographs of the pixel at different focus depths revealed the mechanism of failure was a broken leg apparently caused by significant pixel warping.

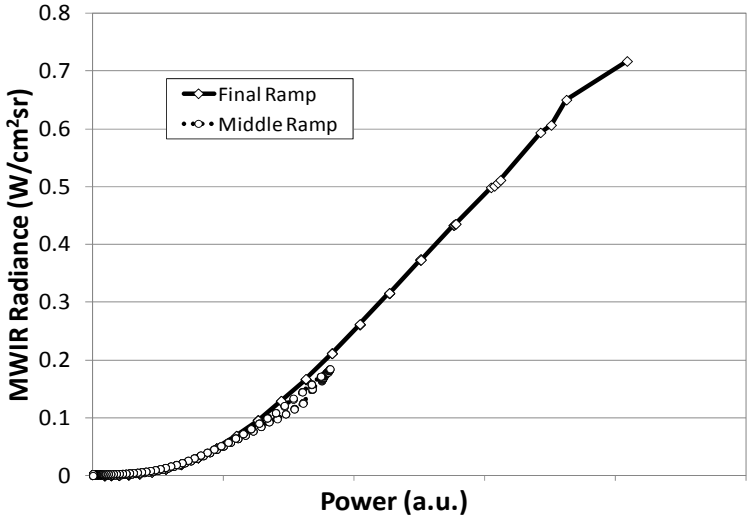

Fig. 7. Radiance vs. applied electrical power.

This finished pixel has no absorber (not included for simplicity) and no reflector (pixel is undercut by ~10 μm), and a slightly smaller fill factor than standard pixel designs, leading to an effective emissivity much lower than a standard pixel. Radiance for a standard design, as in Fig. 1, is expected to be ~ 3.5 X higher. Thus, a pixel fabricated from the same proprietary materials as studied here and including absorber and reflector components, might give good repeatable performance without damage up to a radiance of 3 x 0.7 W/ cm^2-sr, or a MWIR apparent temperature of about 1500 K.

4. SUMMARY

We have designed and fabricated simplified pixels for testing of new materials for high temperature infrared scene projector applications. Fabricated pixels showed no thermal shorts and potential mid-wave infrared apparent temperatures as high as 1500 K.

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